library ieee;

use ieee.std\_logic\_1164.all;

use ieee.std\_logic\_unsigned.all;

use ieee.std\_logic\_arith.all;

entity add\_sub is

port(a,b: in std\_logic\_vector(3 downto 0);

mode,cin,bin: in std\_logic;

cout, bout: out std\_logic;

sum,dif: out std\_logic\_vector(3 downto 0));

end add\_sub;

architecture A\_S of add\_sub is

begin

process(a,b,cin,bin,mode)

variable FORSUM,FORDIF,FORA,FORB,OUTPUT: std\_logic\_vector(4 downto 0);

begin

if mode = '0' then --adder

FORSUM:="00000";

FORSUM(0):=Cin;

FORA(4):='1';

FORA(3 downto 0):=a;

FORB(4):='0';

FORB(3 downto 0):=b;

OUTPUT:=FORA+FORB+FORSUM;

SUM<=OUTPUT(3 downto 0);

Cout<=OUTPUT(4);

DIF<="0000";

else

FORDIF:="00000";

FORDIF(0):=Bin;

FORA(4):='0';

FORA(3 downto 0):=a;

FORB(4):='0';

FORB(3 downto 0):=b;

OUTPUT:=FORA-FORB-FORDIF;

DIF<=OUTPUT(3 downto 0);

Bout<=OUTPUT(4);

SUM<="0000";

end if;

end process;

end a\_S;